IN THE CLAIMS:

Please amend claim 1 to read as follows:

1. (Currently Amended) In a microprocessor having a clock, a program control and a plurality of circuit components comprising registers, at least one arithmetic logic, unit (ALU) having inputs and at least one output, a at least one memory and input/output circuits, the improvement wherein said plurality of components are interconnected on a grid of buses; wherein each of said plurality of components can be switched under program control to be connected to a predetermined selection of one or more of said plurality of components to route data through said grid for processing by said predetermined selection of one or more of said plurality of components; wherein said ~~bus~~ inputs and ~~outputs~~ said at least one output of said ALU are each connected to a separate bus of said grid; and wherein said ALU is operative to receive, process and output data during one microprocessor clock cycle.

2. Canceled.

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3. (Previously Presented) The microprocessor as claimed in claim 1, further comprising a grid connector which includes logic for interconnecting a predetermined one or more of said plurality of components with one or more other components of said plurality of components to said grid.

4. (Previously Presented) The microprocessor as claimed in claim 1, further comprising an instruction set decoder for interpreting the instruction set of said microprocessor into timed signals to said components, a clock for timing operations of said microprocessor and a grid connector which provides logic for interconnecting a predetermined one or more of said plurality of components with one or more other components of said plurality of components to said grid.

5. (Previously Presented) The microprocessor as claimed in claim 1, further comprising at least one further grid of a plurality of further components which are selected from registers, arithmetic logic units, memory, and input/output circuits, and wherein at least a part of said grid is coupled to at least a part of said at least one further grid.

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6. (Previously Presented) The microprocessor as claimed in claim 1, wherein said grid is an X - Y grid having respective X and Y buses and each component connects to one or more of said buses, a switch node is present on each intersecting point of an X and Y bus whereby each switch node provides direct bi-directional connection between said X and Y buses to provide connection of a first one of said components to a second one of said components.

7. (Previously Presented) The microprocessor as claimed in claim 6, wherein connection of said first one of said components to said second one of said components can occur through one or more of said switch nodes to provide X-X, X-Y, Y-Y or Y-X bus connections.

8. (Previously Presented) The microprocessor as claimed in claim 6, wherein a plurality of connections are provided whereby each component can make multiple connections through said grid to one or more of the other components.

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9. (Previously Presented) The microprocessor as claimed in claim 7, wherein a plurality of X-X, X-Y, Y-Y and Y-X bus connections can be made.

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